#10

Attorney Docket No.: 500.36683CX1
Serial No.: 10/025,743

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Hiroki Kanai et al

Serial No: 10/025,743

Filed: December 26, 2001

Title: INFORMATION PROCESSING SYSTEM

Group: 2187

Examiner: Kimberly N. Mayo

APPEAL BRIEF

Assistant Commissioner
for Patents
Washington, D.C. 20231

December 30, 2002

Sir:

This appeal is taken from the final rejection of claims 1-8, 11, 12 and 17-29 as set forth in the final Office Action of September 13, 2002 (hereafter the Office Action). In accordance with 37 C.F.R. § 1.192, applicants address the following items.

REAL PARTY IN INTEREST

The real party in interest is Hitachi, Ltd. of Tokyo, Japan.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

The parent application to the present application issued as U.S. Patent 6,341,335 on January 22, 2002.

STATUS OF CLAIMS

Claims 1-8, 11, 12 and 17-29 have been finally rejected and are on appeal. No claims have been allowed or indicated as allowable.

STATUS OF AMENDMENTS

An Amendment After Final Rejection is being filed simultaneously with this Appeal Brief. It is assumed that this amendment will be entered since it relates to minor formalities. The claims on appeal after entry of this amendment are in Appendix A. The claims on appeal without entry of this amendment are in Appendix B. Both Appendix A and Appendix B contain all claims 1-8, 11, 12 and 17-29.

ISSUES ON APPEAL

I. Whether claims 1, 5, 8, 11, 17-18, 22-23 and 26-27 are unpatentable under 35 U.S.C. § 102(e) over U.S. Patent 5,752,272 to Tanabe.

II. Whether claims 2 and 19-20 are unpatentable under 35 U.S.C. §103(a) over Tanabe in view of U.S. Patent 5,778,422 to Genduso.

III. Whether claims 3-4 and 21 are unpatentable under 35 U.S.C § 103(a) over Tanabe in view of U.S. Patent 5,935,253 to Conary et al. (hereafter Conary).

IV. Whether claims 12 and 28 are unpatentable under 35 U.S.C. §103(a) over Tanabe in view of Genduso, U.S. Patent 5,829,031 to Lynch and Handy, The Cache Memory Book.

V. Whether claims 6 and 24 are unpatentable under 35 U.S.C 103(a) over Tanabe in view of U.S. Patent 5,381,532 to Suzuki.

VI. Whether claims 7 and 25 are unpatentable under 35 U.S.C. § 103(a) over Tanabe in view of U.S. Patent 5,357,618 to Mirza.

VII. Whether claim 21 is unpatentable under 35 U.S.C. § 112, second paragraph.

SUMMARY OF THE INVENTION

As set forth in the present specification, a memory system includes a processor 1, a memory controller 2 and a memory 3. The memory controller 2 controls data transfer between the processor 1 and memory 3. The memory controller 2 divides a memory space viewed from the processor into an instruction code memory area and a data memory area. The memory 3 has a data memory 31 for data storage and an instruction code memory 32 for instruction code storage. See page 9, line 27 – page 10, line 18 of the present specification.

The processor 1 and the memory controller 2 are connected by a system bus 100. The memory controller 2 is connected to data memory 31 by memory bus 101 and the memory controller 2 is connected to instruction code memory 32 by memory bus 102. Memory bus 101 and memory bus 102 are independent of each other. See page 10, lines19 – 22 of the present specification.

The memory controller 2 includes an access judgment circuit 4, a control circuit 5, switch circuits 6 and 9, a direct bus 7 and a buffer memory 8. The access judgment circuit 4 analyzes an access from the processor 1, and divides a memory

read access from the processor 1 into an instruction code access and a data access. The access judgment circuit 4 also judges whether or not the data accessed by the processor 1 is present in the buffer memory 8. See page 11, lines 13-22 of the present specification.

As shown in Figure 2, the access judgment circuit 4 includes a prefetch hit judgment circuit 41 and an instruction fetch detection circuit 42. The prefetch hit judgment circuit includes a prefetch address register 411 for storing therein the address of the prefetched instruction code and a comparator 412 for comparing the address accessed by the processor with the address prefetched by the memory controller. When both addresses coincide with each other, the prefetch hit judgment circuit 41 judges it as a prefetch hit. See page 14, lines 1-17 of the present specification. The prefetched instruction code (from the instruction code memory 32) may be stored in the buffer memory. See page 12, lines 21-23 of the present specification.

The direct bus 7 is a transmission path to transmit read data from the instruction code memory 32 directly to the system bus control circuit 20 without passing through the buffer memory 8. This reduces the overhead time. See page 12, lines 15-20 of the present specification.

The buffer memory 8 temporarily stores an instruction code prefetched from the instruction code memory 32. This reduces the access latency of the processor and increases the fetch speed of the prefetch hit. See page 12, line 21 – page 13, line 7 of the present specification. The buffer memory 8 includes a plurality of buffer

memories having a width equal to the access size of the processor. Data transfer may be carried out in an order requested by the processor in a processor transfer mode. See page 17, lines 17-27 of the present specification.

The control circuit 5 includes a prefetch address generation circuit 51, a prefetch sequencer 52 and a selector 53 as shown in Figure 4. The prefetch address generation circuit 51 generates a prefetch address on the basis of an address anticipated to be next accessed by the processor. The prefetch sequencer 52 executes a memory access and a prefetch from the memory based on information from the system bus control line or access judgment circuit 4. See page 16, lines 7-28 of the present specification.

Figure 6 shows another embodiment of the memory controller. This memory controller 2 includes an instruction decoder circuit 43 and a branching buffer memory 84. The instruction decoder circuit 43 decodes and analyzes an instruction code transferred from the instruction code memory 32 to the memory controller 2. When the instruction decoder circuit 43 detects a branch instruction, the control circuit 5 reads ahead an instruction code at the branch destination into the branching buffer memory 84. In the presence of an instruction code access from the processor, the access judgment circuit 4 judges whether or not it is found in the read-ahead buffer memory 8 or in the branching buffer memory 84. See page 18, lines 2-24 of the present specification.

Figure 7 shows another embodiment of the present invention. The buffer memory and control circuit are included for the instruction code area, the data

memory area and the register area, individually. Switch circuits 61, 62, 63, direct paths 71, 72 and 73 and buffer memories 81, 82 and 83 are provided for each area. When a sequential read access is generated for each area, read-ahead can be done for each buffer memory. See page18, line 25 – page 19, line 23 of the present specification.

An I/O control circuit 503 includes a register 5031 for start and stop instructions of read-ahead. See page 20, lines 1-7; page 29, lines 7-10; and original claim 7 on page 33, last two lines to page 34, first two lines.

The processor 1 includes an L1 (level 1) cache 12. In at least one embodiment, the memory bus 101 may have a transfer performance of twice higher than that of the system bus 100. See page 25, lines 8-28 of the present specification.

The present specification also contains additional embodiments which have not been described above.

GROUPING OF CLAIMS

Each of claims 1-8, 11, 12 and 17-29 stands or falls separately from one another.

ARGUMENT

The present application includes two independent claims, namely claim 1 and claim 18. This claims contain different features as may be evidenced by the specifically claimed features and as may be pointed out below. For ease of illustration, similar types of claims (or claimed features) may be discussed with

respect to each other. This is not an admission that the claims are the same or that they stand and fall together. Rather, this is an attempt to narrow the number of issues and to limit the number of arguments. While arguments may be similar for different claims, it should be understood that different claim features are expressly used.

I. **Claims 1-8, 11, 12 and 17 Define Patentable Subject Matter**

A. Claims 1, 5, 8, 11 and 17 Are Patentable Over Tanabe

Independent claim 1 recites a system bus connecting the processor and the memory controller, and at least two memory buses connecting the memory controller and the memory. The at least two memory buses include a first memory bus for transferring an instruction code and a second memory bus for transferring data. Additionally, independent claim 1 recites that the memory controller includes a buffer, a control circuit and an access judging circuit. The control circuit estimates a most probable address to be accessed next in the memory. The access judging circuit prefetches data stored in the most probable address of the memory into the buffer.

For example, the present specification sets forth that the memory 3 has a data memory 31 for data storage and an instruction code memory 32 for instruction code storage. The memory controller 2 is connected to the data memory 31 by memory bus 101 and the memory controller 2 is connected to the instruction code memory 32 by memory bus 102. The memory buses 101 and 102 are independent of each other. As one advantage of these features, the memory controller may

avoid a contention between the data memory access and instruction code memory access. See page 10, line 6 – page 11, line 7 of the present specification. The specification also discusses that the access judgment circuit 4 divides a memory read access from the processor 1 into an instruction code access and a data code access for discrimination. See page 11, lines13-22.

The Office Action relies on Tanabe to reject claim 1. However, Tanabe does not teach or suggest all the features of independent claim 1. That is, Tanabe's Figure 4 (relied upon in the Office Action) merely shows a micro-processor 3, a memory access control device 1 and a Rambus DRAM 5. The Rambus interface 33 is connected to the Rambus DRAM 5 by a Rambus line RB. See also Tanabe's column 6, lines 39-40.

Tanabe does not teach or suggest at least two memory buses connecting the memory controller and the memory where the at least two memory buses include a first memory bus for transferring an instruction code and a second memory bus for transferring data. Tanabe also does not teach or suggest a control circuit that estimates a most probable address to be accessed next in the memory, and that the access judging circuit prefetches data stored in the most probable address of the memory into the buffer. More specifically, Tanabe shows the Rambus line RB between the DRAM 5 and the Rambus interface 33. At best, this only suggests one connection. Tanabe does not disclose a second bus as in the present application. Independent claim 1 clearly recites at least two memory buses and that the at least two buses connect the memory controller and the memory. The Office Action

attempts to correlate ½ of the Rambus line RB as being a first memory bus and the other ½ of the Rambus line RB as being a second memory bus. The present application is clear regarding the meaning of at least two buses as well as the first memory bus and the second memory bus. These buses are described as being independent of one another. One skilled in the art would clearly understand that the meaning of at least two memory buses does not correlate to a single Rambus line RB. That is, memory buses are more than just simple interconnection between components. The at least two memory bus limitation is further recited as a first memory bus for transferring instruction code and a second memory bus for transferring data. The Office Action does not provide any distinctions between instruction code and data despite the claimed features (and their meaning in the specification). The present application explicitly discusses the use of distinguishing between instruction code and data. These features should be properly interpreted in the claimed features. The Office Action has failed to properly interpret these features.

As noted above, independent claim 1 also recites that the control circuit estimates a most probable address to be accessed next in the memory and that the access judging circuit prefetches data stored in the most probable address of the memory into the buffer. For example, the present application sets forth that control circuit estimates an address to be possibly next accessed on the basis of addresses in the past and to prefetch data stored in the memory into the buffer memory in

Not claimed

accordance with the estimated address. See page 7, lines 10-16; and original claim 14.

Tanabe does not estimate a most probable address to be accessed next and then prefetch data stored in the most probable address of the memory into the buffer. Rather, Tanabe makes a read request to the memory device for the additional block data starting from an address immediately following the last address of the block already stored. See Tanabe's col.10, lines 34-38. Tanabe states that there is a high probability for sooner or later receiving the read out requests for the blocks. See Tanabe's col. 10, lines 39-50. Thus, Tanabe does not estimate a most probable address and then prefetch data stored at the corresponding most probable address. Rather, Tanabe merely reads out an immediately following block of data, which is admitted to possibly not be the most probable. Thus, Tanabe does not teach or suggest these features of the control circuit and the access judging circuit relating to the most probable address.

Tanabe also does not teach or suggest the advantages of the claimed features, namely that since the instruction code memory is separated from the data memory and the memory bus and its control circuit are provided for each of the memories, then contention may be avoided on the memory bus between the instruction code read ahead and the data access. See on page 27, line 26-page 28, line 3 of the present specification.

For at least the reasons set forth above, it is respectfully submitted that Tanabe does not teach or suggest the at least two memory buses connecting the

memory controller and the memory, the at least two memory buses including a first memory bus for transferring an instruction code and a second memory bus for transferring data as recited in independent claim 1. Additionally, Tanabe does not teach or suggest that the control circuit estimates a most probable address to be accessed next in the memory and that the access judging circuit prefetches data stored in the most probable address of the memory into the buffer as recited in independent claim 1.

Dependent claim 5 recites that the memory controller further comprises a plurality of buffers, wherein the control circuit transfers data already stored in the plurality of buffers to the processor in an order different from an address order. The Office Action asserts that Tanabe (registers 38A-38D, column 13, lines 51-55 and column 16, lines 50-53) discloses this feature since each memory is accessed independently. However, this does not teach or suggest transferring data stored in buffers to the processor in an order different from an address order. Tanabe does not suggest transferring in an order different from an address order. Absent some suggestion, it is improper to suggest that Tanabe discloses this feature.

Dependent claim 8 recites that the control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into the buffer. The Office Action relies on Tanabe's col. 7, lines 28-52 for these features. However, Tanabe does not disclose prefetching data already stored at a pre-specified address. That is, Tanabe does not suggest prefetching data from a pre-specified address. As indicated above, Tanabe prefetches block data starting from the address

immediately following the last address of the block data already stored. See Tanabe's column 10, lines 34-38.

Dependent claim 11 recites that the processor had an internal cache, and the control circuit is controlled to prefetch data having a data size of twice or more a line size of the internal cache into the buffer. Tanabe does not teach or suggest these features of dependent claim 11 in combination with the additional features of claim 1.

Dependent claim 17 recites that the access judging circuit prefetches the instruction code from the memory along the first memory bus and into the buffer. As indicated above, Tanabe does not disclose a first memory bus or prefetching instruction code. Tanabe does not even recognize instruction code. Thus, Tanabe does not suggest these features of claim 17 in combination with the additional features of claim 1.

B. Claims 2-4, 6, 7 and 12 Are Patentable Over the Alleged Combinations

Dependent claim 2 recites that the memory controller comprises a direct path for transmitting data directly to the processor from the memory therethrough. The Office Action agrees that Tanabe does not disclose this feature. The Office Action then relies on Genduso's Figure 1 (element 18) to show this feature. However this does not show the claimed direct path within the memory controller. Genduso's Figure 1 merely shows a memory controller between the processor and the memory. Additionally, the Office states that it would have been obvious to modify Tanabe (allegedly transferring data from memory to a buffer and then to the processor from

the buffer) based on Genduso. Even if Genduso taught this feature, this modification would be improper. That is, this alleged modification destroys Tanabe's express purpose of using buffers (by allegedly avoiding the buffers). This modification would also fail to meet all the features of claim 1 from which claim 2 depends.

Dependent claim 12 recites that the memory is divided into a first memory for storing therein the instruction code to be executed on the processor and a second memory for storing therein operand data, wherein the access judging circuit for judging whether the memory access from said processor is an access to the first memory or an access to the second memory, the memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and the control circuit is controlled to prefetch the instruction code into the first buffer memory according to a judgment of the access judging circuit or to prefetch the operand data into the second buffer memory. As such, this claim sets forth a unique correlation between a first memory, a second memory, a first buffer memory and a second buffer memory. The Office Action relies on four separate references to find the claimed features without any basis in the prior art. In particular, the Office Action relies on Lynch for the claimed first memory and second memory but relies on Genduso for the claimed first buffer memory and second buffer memory. These references (and Tanabe and Handy) do not teach or suggest the correlation between these elements especially when it is based on an access judging circuit for judging whether the memory access from the

processor is an access to the first memory or an access to the second memory. The Office Action has merely cited specific areas of different references and attempts to combine them without any basis. As such, this combination is improper and does not suggest the features of claim 16.

Dependent claim 7 recites that the memory controller has a register for instructing start or stop of the prefetch to the buffer. The Office Action agrees that Tanabe does not disclose this feature. The Office Action asserts Mirza teaches these concepts, citing Mirza's column 2, lines 60-68 and column 3, lines 5-12. At best, Mirza merely discloses registers. However, both the register 30 and the cache 18 are included inside the processor 10 and are not included within a separate memory controller. See column 4, line 62-column 5, line 10. That is, claim 7 recites that the memory controller has a register. Mirza does not disclose a memory controller. Accordingly, the combination of Tanabe and Mirza does not teach or suggest the feature to claim 7. The alleged combination also does not suggest these features of claim 7 in combination with the additional features of claim 1.

Dependent claim 3 recites that the memory stores the instruction code to be executed on the processor therein, and the control circuit prefetches the instruction code into the buffer. The Office Action agrees that Tanabe does not explicitly disclose prefetching instructions and data. The Office Action relies on Conary to show a cache 201 that stores instructions and data. However, this combination does not suggest the features of claim.3 in combination with the additional features of claim 1.

Dependent claim 4 recites that the memory stores therein the instruction code to be executed on the processor and operand data, and the control circuit prefetches the instruction code and the operand data into the buffer. The Office Action agrees that Tanabe does not explicitly disclose prefetching instructions and data. The Office Action relies on Conary to show a cache 201 that stores instructions and data. However, this combination does not suggest the feature of claim 4 in combination with the additional features of claim 1.

Dependent claim 6 recites the memory controller has an instruction decoder and a branching buffer, and the control circuit, when the instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into the branching buffer and, when an access is made from the processor to the instruction code, judges whether or not the instruction code hits data within the buffer and the branching buffer. The Office Action agrees that Tanabe does not explicitly disclose these features. The Office Action relies on Suzuki to show these features. However, this combination does not suggest theses features of claim 6 in combination with the additional features of claim 1.

II. **Claims 18-29 Define Patentable Subject Matter**

Claims 18-29 differ from claims 1-8, 11, 12 and 17. The features of these claims are set forth below. Each of claims 18-29 stands and falls separately from each other and from each of claims 1-8, 11, 12 and 17 (as the claimed features differ).

A. Claims 18, 22-23, 26-27 and 29 Are Patentable Over Tanabe

Independent claim 18 recites a first memory bus connecting the memory controller and the memory and a second memory bus connecting the memory controller and the memory. Claim 18 further recites that the memory controller includes a control circuit to estimate a most probable address to be accessed next in the memory and an access judging circuit to prefetch data stored in the most probable address of the memory to the buffer. For at least similar reasons as set forth above with respect to claim 1, Tanabe does not teach or suggest these features of independent claim 18.

Dependent claim 22 recites that the memory stores therein instruction code to be executed on the processor and operand data, and the control circuit prefetches the instruction code from the memory and along the first memory bus to the buffer and the control circuit prefetches the operand data from the memory and along the second memory bus to the buffer. For at least similar reasons as set forth above, Tanabe does not teach or suggest these features of claim 22. Tanabe does not relate to prefetching instruction code along a first memory bus and prefetching operand data along a second memory bus.

Dependent claim 23 recites the memory controller further comprises a plurality of buffers, wherein the control circuit transfers data already stored in the plurality of buffers to the processor in an order different from an address order. For at least similar reasons as set forth above with respect to claim 5, Tanabe does not

teach or suggest these features of claim 23 in combination with the additional features of claim 18.

Dependent claim 26 recites that the control circuit is controlled in an initial state to prefetch data already stored at a pre-specified address into the buffer. For at least similar reasons as set forth above with respect to claim 8, Tanabe does not teach or suggest these features of claim 26 in combination with the additional features of claim 18.

Dependent claim 27 recites that the processor includes an internal cache, and the control circuit prefetches data having a data size of twice or more a line size of the internal cache into the buffer. For at least similar reasons as set forth above with respect to claim 11, Tanabe does not teach or suggest these features of claim 27 in combination with the additional features of claim18.

Dependent claim 29 recites the access judging circuit prefetches instruction code from the memory along the first memory bus and into the buffer. The Office Action never addresses this claim. For at least similar reasons as set forth above with respect to claim 17, Tanabe and does not teach or suggest these features of claim 29 in combination with the additional features of claim 18

B. Claims 19-21, 24-25 and 28 Are Patentable Over The Alleged Combinations

Dependent claim 19 recites that the memory controller comprises a direct path for transmitting data directly to the processor from the memory therethrough.

For at least similar reasons as set forth above with respect to claim 2, Tanabe and Genduso do not teach or suggest all the features of claim 19 in combination with the additional features of claim 18.

Dependent claim 20 further depends from claim 19 and additionally recites the memory access from said processor hits data within the buffer, the control circuit transfers the data to the processor, and when the memory access from said processor fails to hit data within the buffer, the control circuit transfers data within the memory to the processor via the direct path. For at least the reasons set forth above, Tanabe and Genduso do not teach or suggest all the features of claim 20 in combination with the additional features of claim 18.

Dependent claim 25 recites the memory controller includes a register for instructing start or stop of a prefetch to the buffer. For at least the reasons set forth above with respect to claim 25, Tanabe and Mirza do not teach or suggest all the features of claim 25 in combination with the additional features of claim 18.

Dependent claim 28 recites that the memory is divided into a first memory for storing therein the instruction code to be executed on the processor and a second memory for storing therein operand data, wherein the access judging circuit judges whether the memory access from the processor is an access to the first memory or an access to the second memory, the memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data, and the control circuit prefetches the instruction code to the first buffer memory according to a judgment of the access judging circuit or prefetches

the operand data to the second buffer memory. For at least the reasons set forth above with respect to claim 12, Tanabe, Genduso, Lynch and Handy do not teach or suggest all the features of claim 28 in combination with the additional features of claim 18.

Dependent claim 21 recites that the memory stores instruction code to be executed on the processor therein, and the control circuit prefetches the instruction code from the memory along the first memory bus to the buffer. For at least similar reasons as set forth above with respect to claim 3, Tanabe and Conary do not teach or suggest all the features of claim 21 in combination with the additional features of claim 18.

Dependent claim 24 recites that the memory controller includes an instruction decoder and a branching buffer, and when the instruction decoder detects a branch instruction, the control circuit prefetches an instruction code as a branch destination to the branching buffer and, when an access is made from the processor to the instruction code, the control circuit judges whether or not the instruction code hits data within the buffer and the branching buffer. For at least the reasons set forth above with respect to claim 6, Tanabe and Suzuki do not teach or suggest all the features of claim 24 in combination with the additional features of claim 18.

III. **Claim 21 is Definite**

The Office Action rejected claim 21 under 35 U.S.C. 112, second paragraph. It is respectfully submitted that the amendment to claim 21 in the simultaneously

filed Amendment After Final Rejection obviates the grounds for rejection under 35 U.S.C. § 112, second paragraph.

CONCLUSION

It is respectfully submitted that the above arguments show that each of the claims are patentable over the cited references. Based at least on these reasons, it is respectfully submitted that each of claims 1-8, 11, 12 and 17-29 defines patentable subject matter. Applicants request that the rejections set forth in the September 13 Office Action be withdrawn.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, L.L.P.

David C. Oren

Attachments:
Appendix A
Appendix B

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 North Seventeenth Street, Suite 1800
Arlington, VA 22209
Phone: (703)312-6600
Fax: (703) 312-6666

APPENDIX A

1. (Twice Amended) An information processing system comprising:

a processor;

a memory;

a memory controller;

a system bus connecting said processor and said memory controller; and;

at least two memory buses connecting said memory controller and said memory, said at least two memory buses comprising:

a first memory bus for transferring an instruction code, and

a second memory bus for transferring data,

said memory controller comprising:

a buffer,

a control circuit, and

an access judging circuit, wherein;

said control circuit estimates a most probable address to be accessed next in said memory, and

said access judging circuit prefetches data stored in said most probable address of the memory into the buffer.

2. (Twice Amended) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

3. (Twice Amended) An information processing system according to claim 1, wherein said memory stores said instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer.

4. (Twice Amended) An information processing system according to claim 1, wherein said memory stores therein said instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and said operand data into said buffer.

5. (Twice Amended) An information processing system according to claim 1, wherein said memory controller further comprising a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

6. (Amended) An information processing system according to claim 1, wherein said memory controller has an instruction decoder and a

branching buffer, and said control circuit, when said instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into said branching buffer and, when an access is made from said processor to the instruction code, judges whether or not the instruction code hits data within said buffer and said branching buffer.

7. (Amended) An information processing system according to claim 1, wherein said memory controller has a register for instructing start or stop of the prefetch to said buffer.

8. (Amended) An information processing system according to claim 1, wherein said control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into said buffer.

11. (Amended) An information processing system according to claim 1, wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said internal cache into said buffer.

12. (Amended) An information processing system according to claim 1, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit for

judging whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and said control circuit is controlled to prefetch the instruction code into said first buffer memory according to a judgment of said access judging circuit or to prefetch the operand data into said second buffer memory.

17. An information processing system according to claim 1, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.

18. An information processing system comprising:

processor;

a memory;

a memory controller;

a system bus connecting said processor and said memory controller;

a first memory bus connecting said memory controller and said memory; and

a second memory bus connecting said memory controller and said memory;

said memory controller comprising:

a buffer;

a control circuit to estimate a most probable address to be accessed next in said memory; and

an access judging circuit to prefetch data stored in said most probable address of the memory to the buffer.

19. An information processing system according to claim 18, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

20. An information processing system according to claim 19, wherein when the memory access from said processor hits data within said buffer, said control circuit transfers the data to the processor, and when the memory access from said processor fails to hit data within said buffer, said control circuit transfers data within said memory to said processor via said direct path.

21. An information processing system according to claim 18, wherein said memory stores instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code from the memory along the first memory bus to said buffer.

22. An information processing system according to claim 18, wherein said memory stores therein instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code from the memory and along the first memory bus to said buffer and said control circuit prefetches the operand data from the memory and along the second memory bus to said buffer.

23. An information processing system according to claim 18, wherein said memory controller further comprises a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

24. An information processing system according to claim 18, wherein said memory controller includes an instruction decoder and a branching buffer, and when said instruction decoder detects a branch instruction, said control circuit prefetches an instruction code as a branch destination to said branching buffer and, when an access is made from said processor to the instruction code, said control circuit judges whether or not the instruction code hits data within said buffer and said branching buffer.

25. An information processing system according to claim 18, wherein said memory controller includes a register for instructing start or stop of a prefetch to said buffer.

26. An information processing system according to claim 18, wherein said control circuit is controlled in an initial state to prefetch data already stored at a pre-specified address into said buffer.

27. An information processing system according to claim 18, wherein said processor includes an internal cache, and said control circuit prefetches data having a data size of twice or more a line size of said internal cache into said buffer.

28. An information processing system according to claim 18, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit judges whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data, and said control circuit prefetches the instruction code to said first buffer memory according to a judgement of said access judging circuit or prefetches the operand data to said second buffer memory.

29.. An information processing system according to claim 18, wherein said access judging circuit prefetches instruction code from said memory along said first memory bus and into the buffer.

APPENDIX B

1. (Twice Amended) An information processing system comprising:

a processor;

a memory;

a memory controller;

a system bus connecting said processor and said memory controller; and;

at least two memory buses connecting said memory controller and said memory, said at least two memory buses comprising:

a first memory bus for transferring an instruction code, and

a second memory bus for transferring data,

said memory controller comprising:

a buffer,

a control circuit, and

an access judging circuit, wherein;

said control circuit estimates a most probable address to be accessed next in said memory, and

said access judging circuit prefetches data stored in said most probable address of the memory into the buffer.

2. (Twice Amended) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

3. (Twice Amended) An information processing system according to claim 1, wherein said memory stores said instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer.

4. (Twice Amended) An information processing system according to claim 1, wherein said memory stores therein said instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and said operand data into said buffer.

5. (Twice Amended) An information processing system according to claim 1, wherein said memory controller further comprising a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

6. (Amended) An information processing system according to claim 1, wherein said memory controller has an instruction decoder and a

branching buffer, and said control circuit, when said instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into said branching buffer and, when an access is made from said processor to the instruction code, judges whether or not the instruction code hits data within said buffer and said branching buffer.

7. (Amended) An information processing system according to claim 1, wherein said memory controller has a register for instructing start or stop of the prefetch to said buffer.

8. (Amended) An information processing system according to claim 1, wherein said control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into said buffer.

11. (Amended) An information processing system according to claim 1, wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said internal cache into said buffer.

12. (Amended) An information processing system according to claim 1, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit for

judging whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and said control circuit is controlled to prefetch the instruction code into said first buffer memory according to a judgment of said access judging circuit or to prefetch the operand data into said second buffer memory.

17. An information processing system according to claim 1, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.

18. An information processing system comprising:

processor;

a memory;

a memory controller;

a system bus connecting said processor and said memory controller;

a first memory bus connecting said memory controller and said memory; and

a second memory bus connecting said memory controller and said memory;

said memory controller comprising:

a buffer;

a control circuit to estimate a most probable address to be accessed next in said memory; and

an access judging circuit to prefetch data stored in said most probable address of the memory to the buffer.

19. An information processing system according to claim 18, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

20. An information processing system according to claim 19, wherein when the memory access from said processor hits data within said buffer, said control circuit transfers the data to the processor, and when the memory access from said processor fails to hit data within said buffer, said control circuit transfers data within said memory to said processor via said direct path.

21. An information processing system according to claim 18, wherein said memory stores instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code from the memory pad along the first memory bus to said buffer.

22.. An information processing system according to claim 18, wherein said memory stores therein instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code from the memory and along the first memory bus to said buffer and said control circuit prefetches the instruction code from the memory and along the second memory bus to said buffer.

23. An information processing system according to claim 18, wherein said memory controller further comprises a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

24. An information processing system according to claim 18, wherein said memory controller includes an instruction decoder and a branching buffer, and when said instruction decoder detects a branch instruction, said control circuit prefetches an instruction code as a branch destination to said branching buffer and, when an access is made from said processor to the instruction code, said control circuit judges whether or not the instruction code hits data within said buffer and said branching buffer.

25. An information processing system according to claim 18, wherein said memory controller includes a register for instructing start or stop of a prefetch to said buffer.

26. An information processing system according to claim 18, wherein said control circuit is controlled in an initial state to prefetch data already stored at a pre-specified address into said buffer.

27. An information processing system according to claim 18, wherein said processor includes an internal cache, and said control circuit prefetches data having a data size of twice or more a line size of said internal cache into said buffer.

28. An information processing system according to claim 18, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit judges whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data, and said control circuit prefetches the instruction code to said first buffer memory according to a judgement of said access judging circuit or prefetches the operand data to said second buffer memory.

29.. An information processing system according to claim 18, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.